

NTE2532 Integrated Circuit NMOS, 32K EPROM, 300ns

Description:

The NTE2532 is a 32,768-bit, ultraviolet-light-erasable, electrically-programmable read-only memory in a 24-Lead DIP type package. This device is fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be directly driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus.

Since the NTE2532 operates from a single +5V supply (in the read mode), it is ideal for use in microprocessor systems. One other (+25V) supply is needed for programming but all programming signals are TTL level, requiring a single 10ms pulse. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 41 seconds.

Features:

- Organization: 4096 x 8
- Single +5V Power Supply
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time: 300ns
- 8-Bit Output for Use in Microprocessor Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- Low Power Dissipation:
 - Active – 400mW Typical
 - Standby – 100mW Standby
- Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required

Absolute Maximum Ratings: ($T_A = 0^\circ$ to $+70^\circ\text{C}$, Note 1 unless otherwise specified)

Supply Voltage (Note 2), V_{CC}	–0.3V to +7V
Supply Voltage (Note 2), V_{PP}	–0.3V to +28V
All Input Voltages (Note 1)	–0.3V to +7V
Output Voltage (Operating, with Respect to V_{SS})	–0.3V to 7V
Operating Ambient Temperature Range, T_A	0° to $+70^\circ\text{C}$
Storage Temperature Range, T_{stg}	-55° to $+150^\circ\text{C}$

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operation Conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2. Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage, V_S (substrate).

Recommended Operating Conditions:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	Note 3	4.75	5.0	5.25	V
	V_{PP}	Note 4	–	V_{CC}	–	V
	V_{SS}		–	0	–	V
High Level Input Voltage	V_{IH}		2	–	$V_{CC}+1$	V
Low Level Input Voltage	V_{IL}		–0.1	–	+0.8	V
Read Cycle Time	$t_{c(rd)}$		300	–	–	ns
Operating Ambient Temperature	T_A		0	–	70	°C

Note 3. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP} . The device must not be inserted into or removed from the board when V_{PP} is applied.

Note 4. V_{PP} can be connected to V_{CC} directly (except in the programming mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 25V ($\pm 1V$).

Electrical Characteristics: (Over full range of recommended operating conditions)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Output Voltage	V_{OH}	$I_{OH} = -400\mu A$	2.4	–	–	V
Low Level Output Voltage	V_{OL}	$I_{OL} = 2.1mA$	–	–	0.45	V
Input Current (Leakage)	I_I	$V_I = 0V$ to 5.25V	–	–	± 10	μA
Output Current (Leakage)	I_O	$V_O = 0.4V$ to 5.25V	–	–	± 10	μA
V_{PP} Supply Current	I_{PP1}	$V_{PP} = 5.25V$, $PD/\overline{PGM} = V_{IL}$	–	–	12	mA
V_{PP} Supply Current (During Program Pulse)	I_{PP2}	$PD/\overline{PGM} = V_{IL}$	–	–	30	mA
V_{CC} Supply Current (Standby)	I_{CC1}	$PD/\overline{PGM} = V_{IH}$	–	20	–30	mA
V_{CC} Supply Current (Active)	I_{CC2}	$PD/\overline{PGM} = V_{IL}$	–	80	160	mA

Capacitance: (Over recommended voltage and operating ambient temperature range, $f = 1MHz$, Note 5, Note 6)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance	C_i	$V_I = 0V$, $f = 1MHz$	–	4	6	pF
Output Capacitance	C_o	$V_O = 0V$, $f = 1MHz$	–	8	12	pF

Note 5. All typical values are at $T_A = +25^\circ C$ and nominal voltages.

Note 6. Capacitance measurements are made on a sample basis only.

Switching Characteristics: (Over full range of recommended operating conditions, Note 5, Note 8)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Access Time from Address	$t_{a(A)}$	$C_L = 100pF$, 1 Series 74 TTL Load, $t_r \leq 20ns$, $t_f \leq 20ns$, Note 8, Note 9	–	–	300	ns
Access Time from PD/\overline{PGM}	$t_{a(PR)}$		–	–	300	ns
Output Data Valid after Address Change	$t_{v(A)}$		0	–	–	ns
Output Disable Time from PD/\overline{PGM} (Note 7)	t_{dis}		–	–	100	ns

Note 5. All typical values are at $T_A = +25^\circ C$ and nominal voltages.

Note 7. Value calculated from 0.5V delta to measured output level

Note 8. Timing measurement reference levels: inputs 0.8V and 2V, outputs 0.65V and 2.2V.

Note 9. Common test conditions apply for t_{dis} except during programming. For $t_{a(A)}$ and t_{dis} , $PD/\overline{PGM} = V_{IL}$.

Recommended Timing Requirement for Programming: ($T_A = +25^{\circ}\text{C}$, Note 8, Note 10)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Pulse Duration, Program Pulse	$t_{w(PR)}$		9	–	–	ms
Rise Time, Program Pulse	$t_{r(PR)}$		5	–	–	ns
Fall Time, Program Pulse	$t_{f(PR)}$		5	–	–	ns
Address Setup Time	$t_{su(A)}$		2	–	–	μs
Data Setup Time	$t_{su(D)}$		2	–	–	μs
Setup Time for V_{PP}	$t_{su(VPP)}$		0	–	–	ns
Address Hold Time	$t_{h(A)}$		2	–	–	μs
Data Hold Time	$t_{h(D)}$		2	–	–	μs
Program Pulse Hold Time	$t_{h(PR)}$		0	–	–	ns
V_{PP} Hold Time	$t_{h(VPP)}$		2	–	–	μs

Note 8. Timing measurement reference levels: inputs 0.8V and 2V, outputs 0.65V and 2.2V.

Note 10. Typical values are at nominal voltages.

Operation:

Function (Pins)	Mode				
	Read	Output Disable	Power Down	Start Programming	Inhibit Programming
PD/ $\overline{\text{PGM}}$ (20)	V_{IL}	V_{IH}	V_{IH}	Pulsed V_{IH} to V_{IL}	V_{IH}
V_{PP} (21)	+5V	+5V	+5V	+25V	+25V
V_{CC} (24)	+5V	+5V	+5V	+5V	+5V
Q (9 to 11, 13 to 17)	Q	High-Z	High-Z	D	High-Z

Read/Out Disable

When the outputs of two or more NTE2532s are connected on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. The device whose output is to be read should have a low-level TTL signal applied to the PD/ $\overline{\text{PGM}}$ pin. Output data is accessed at pins Q1 through Q8.

Power Down

Active power dissipation can be cut by over 70% by applying a high TTL signal to the PD/ $\overline{\text{PGM}}$ pin. In this mode all outputs are in a high-impedance state.

Erase

Before programming, the NTE2532 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light having a wavelength of 253.7nm (2537 angstroms). The recommended minimum exposure dose (UV intensity time exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12 milliwatt per square centimeter filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are in the “1” state (assuming high-level output corresponds to logic “1”). It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore when using the NTE2532, the window should be covered with an opaque label.

Start Programming

After erasure (all bits in logic “1” state), logic “0’s” are programmed into the desired locations. A “0” can be erased only by ultraviolet light. The programming mode is achieved when V_{PP} is 25V. Data is presented in parallel (8 bits) on pins Q1 through Q8. Once addresses and data are stable, a 10-millisecond TTL low-level pulse should be applied to the $\overline{\text{PGM}}$ pin at each address location to be programmed. Maximum pulse width is 44 milliseconds. Locations can be programmed in any order. Several NTE2532s can be programmed simultaneously when the devices are connected in parallel.

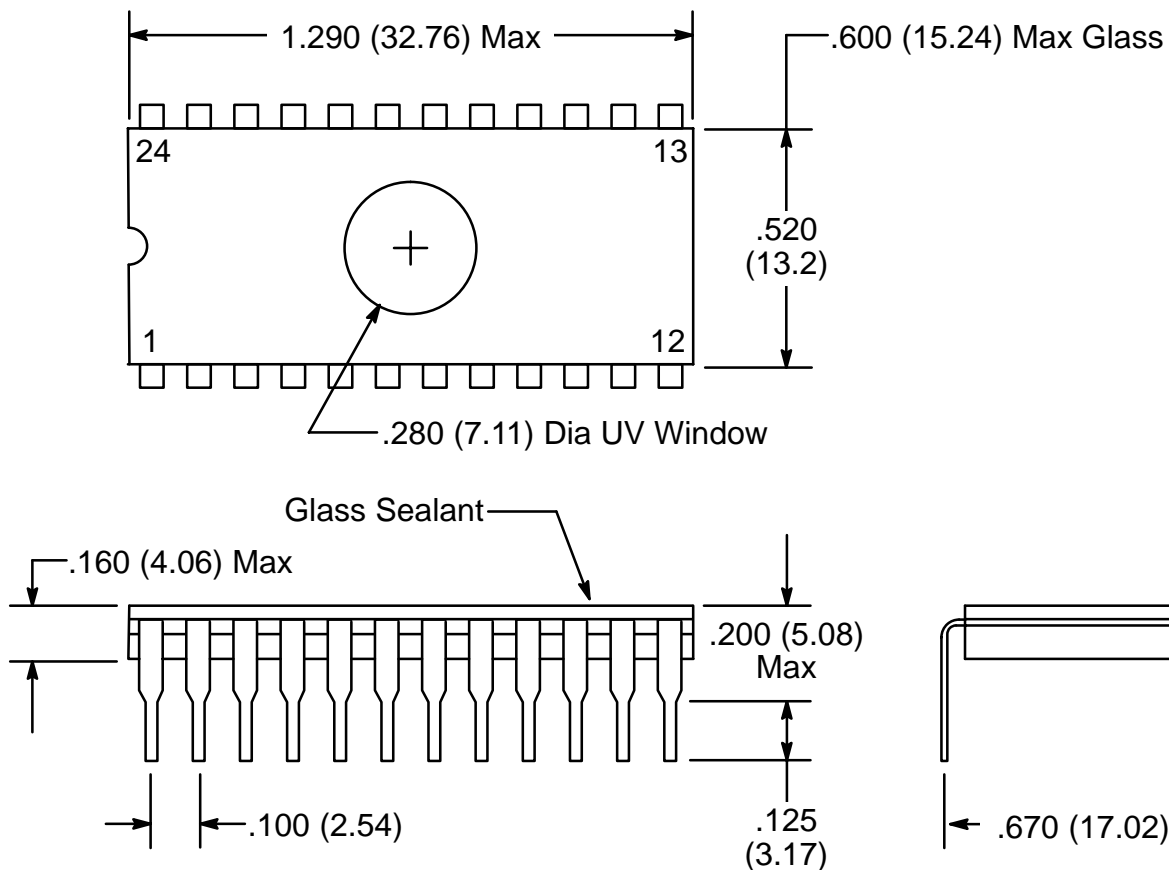
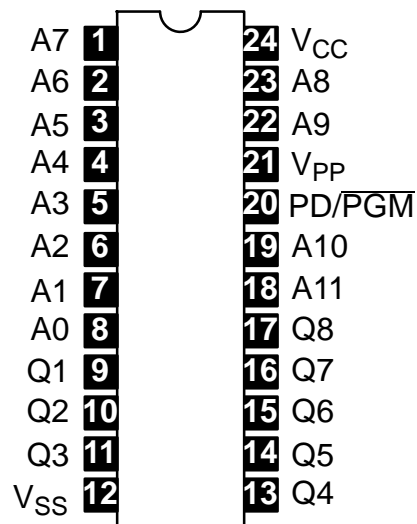
Inhibit Programming

When two or more devices are connected in parallel, data can be programmed into all devices or only chosen devices. Any NTE2532 not intended to be programmed should have a high level applied to $\overline{\text{PD/PGM}}$.

Programming Verification

The NTE2532 program verification is simply the read operation, which can be performed as soon as V_{PP} returns to +5V ending the program cycle.

Pin Connection Diagram



Copyright © Each Manufacturing Company.

All Datasheets cannot be modified without permission.

This datasheet has been download from :

www.AllDataSheet.com

100% Free DataSheet Search Site.

Free Download.

No Register.

Fast Search System.

www.AllDataSheet.com